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Attorney for Appellant

PATENT
Docket No. SJO920030029US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant: | David F. Hepner et. al | ) |
| Serial No.: | 10/671,251 | ) |
| Filed: | September 25, 2003 | ) Group Art Unit: 2116 |
| For: | **HARDWARE CPU UTILIZATION METER FOR A MICROPROCESSOR** | ) |
| Examiner: | James F. Sugent | ) |

## APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner:

The Appellants filed a timely Notice of Appeal on January 8, 2007, which was filed in response to the Final Office Action mailed September 6, 2006 and the Advisory Action mailed November 21, 2006. Appellant appeals the rejection of pending Claims 1-20.

This Appeal Brief is being filed under the provisions of 37 C.F.R. § 41.37. The filing fee set forth in 37 C.F.R. § 41.20(b)(2) of $500.00 is submitted herewith. The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or to credit any overpayment, to Deposit Account No. 09-0466.

**1. REAL PARTY IN INTEREST**

The real party in interest is the assignee, International Business Machines Corporation, Armonk, New York.

**2. RELATED APPEALS AND INTERFERENCES**

There are no related appeals, interferences, or judicial proceedings.

**3. STATUS OF CLAIMS**

Claims 1-20 stand rejected. Claims 1-4 and 11-14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 2004/0059956 to Chakravarthy et. al (hereinafter "Chakravarthy"). Claims 5-10 and 15-20 stand rejected under 35 U.S.C. § 103(a). In particular, claims 5-10 and 15-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chakravarthy in view of U.S. Patent No. 2004/0098631 to Terrell, II (hereinafter "Terrell").

According to the Advisory Action mailed April 26, 2005, the claims remain rejected as set forth in the final rejection. The Advisory Action found Appellants' arguments unpersuasive. Appellant appeals the rejection of Claims 1-20.

**4. STATUS OF AMENDMENTS**

No amendments have been submitted subsequent to the Final Office Action mailed September 6, 2006.

**5. SUMMARY OF CLAIMED SUBJECT MATTER**

The present invention provides a hardware based solution to CPU utilization and power management by throttling back microprocessors not currently in use and speeding up needed CPU capacity, for example by reducing the clock speed of the CPU and other logic when the CPU is idle. See Specification, ¶ 5.

Embodiments of the present invention include a microprocessor system and method of operating a microprocessor system. See Claims 1-20. The microprocessor system of Claim 1 includes a clock providing a CLK signal to the CPU, a counter counting clock pulses to the CPU, and a monitor, wherein the clock is adapted to provide a CLK signal to the counter when a software task is running on the CPU, said counter adapted to count the number of clock pulses since a RESET; the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU; and the monitor is adapted to store the value in the counter immediately prior to the last RESET. See Fig. 1 for an example.

Claims 2-10 include further embodiments of the present invention. In Claim 2, the CPU is adapted to block a RESET signal to the counter when a software task is running on the CPU. In Claim 3, the CPU is adapted to continuously pass CLK signals to the counter when a software task is running on the CPU. In Claim 4, the CPU is adapted to pass a RESET signal to the counter when a software task is not running on the CPU. In Claim 5, the monitor is adapted to output a control signal responsive to monitor content.

Claims 6-10 depend from Claim 5. In Claim 6, the monitor is adapted to output a power control signal responsive to monitor content. In Claim 7, the monitor is adapted to output a function control signal responsive to monitor content. In Claim 8, the monitor is adapted to output a clock control signal responsive to monitor content. In Claim 9, the monitor is adapted to output a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold. In Claim 10, the monitor is adapted to output a control signal reducing clock pulse input to the CPU responsive to count content when the monitor is below a threshold.

Method Claims 11-20 include substantially the same embodiments as those described above with respect to Claims 1-10.

## 6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether the Examiner failed to establish a *prima facie* case of anticipation under 35 U.S.C. § 102(e) for Claims 1-4 and 11-14 where the limitations of the claims are not taught or suggested within Chakravarthy.

II. Whether the Examiner failed to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a) for Claims 5-10 and 15-20 where the limitations of the claims are not taught or suggested within the combination of Chakravarthy and Terrell.

## 7. ARGUMENT

**I. The Examiner failed to establish a *prima facie* case of anticipation under 35 U.S.C. § 102(e) because Chakravarthy does not teach every element of Claims 1-4 and 11-14.**

**Claims 1-4 and 11-14**

A. Independent Claims 1 and 11

Appellant respectfully submits that independent Claim 1 is representative of the novel subject matter of Claim 14. Appellant also submits that Claim 1 is patentable over Chakravarthy because Chakravarthy fails to teach each element of Claim 1. Claim 1 states:

> A microprocessor system comprising a CPU, a clock providing a CLK signal to the CPU, a counter counting clock pulses to the CPU, and a monitor, wherein the clock is adapted to provide a CLK signal to the counter when a software task is running on the CPU, said **counter adapted to count the number of clock pulses since a RESET**; the **CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU**; and the monitor is adapted to store the value in the counter immediately prior to the last RESET.

(emphasis added).

"Anticipation under 35 U.S.C. §102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention." *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 20, 57 USPQ2d 1057, 1061 (Fed. Cir. 2000). An anticipation under section 102 is proper only if the reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

With regard to the rejection of independent Claims 1 and 11, Applicant respectfully submits that these claims are patentable over the cited reference, because Chakravarthy fails to teach each and every element set forth in Claims 1 and 11. Specifically Chakravarthy fails to teach the recited element wherein "the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running."

To support the rejection of claims 1 and 11, the Final Office Action suggests that the signal (PMCPUCLKUNHALTED# 222) disclosed in Chakravathy is the equivalent of the RESET signal in claims 1 and 11 of the present invention. See Office Action, September 6, 2006, p. 2. The Final Office Action further states that Chakravarthy anticipates the element of Claims 1 and 11 wherein "the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running" by disclosing that a "counter within the performance monitor 204 does not count the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is de-asserted." See Office Action, September 6, 2006, pp. 2-3 (citing Chakravarthy paragraph 28). Applicant respectfully disagrees with the Office Action's characterization of the cited reference.

The signal (PMCPUCLKUNHALTED# 222) is not the equivalent of the RESET signal claimed in the present invention. The signal (PMCPUCLKUNHALTED# 222) acts as an enabling signal in Chakravarthy such that a counter continues to increment only when that signal is asserted, but the signal (PMCPUCLKUNHALTED# 222) does not cause the counter to reset regardless of whether or not it is asserted. Paragraph 28. Conversely, the RESET signal in the present invention may "reset[] the counter, 15, to zero, and set[] the monitor, 17 to the level of the counter, 15, immediately prior to the RESET signal." See Application p. 4, lines 9-12 and lines 25-30. A signal that enables a counter to count and a signal that resets a counter to zero are patentably distinguishable. One that is skilled in the art will readily recognize the difference between a RESET signal and an ENABLE signal with regard to microprocessors. Disregarding

these patentable differences also disregards any benefits, advances, or improvements made possible by the claimed invention. Such benefits may include "avoid[ing] an additional set or layer of software tasks to monitor CPU utilization," by employing a hardware solution to reduce heat dissipation and battery drain. See Specification, p. 3, lines 16-29. Therefore, Applicants respectfully assert that Claims 1 and 11 are patentable over Chakravarthy because Chakravarthy fails to show exactly what is claimed in each and every limitation of the claims.

A close reading of Chakravarthy further demonstrates the importance of this distinction. Chakravarthy utilizes an additional system timer to properly function. See Figures 5 and 6 and paragraphs 36-39. That invention initializes a timer and begins counting the number of clock cycles used by the microprocessor. Then, after a preset sampling time period ends, the timer is stopped and calculations are made to determine how many clock cycles were used by the microprocessor during the sampling period. See Figures 5 and 6 and paragraphs 36-39. The present invention on the other hand, directly utilizes a count value to continuously enhance the efficiency of the system by adjusting control signals based on the count value. See Application Figure 2 and the text generally.

For example, Fig. 2 depicts one example of why the RESET signal of the present invention differs from the enabling signal PMCPUCLKUNHALTED# 222. Notice that the count value is automatically reset whenever a software task is not running on the CPU as recited in Claim 1. Thus, the higher the count value, the longer the CPU has been in continuous use. For example, a CPU that is not being utilized as often will be frequently reset such that the count value remains below a particular threshold, and conversely, if CPU usage is very high, the count value might exceed a particular threshold. Subsequently, the clock or CPU may be adjusted or reconfigured automatically and directly based on the count value. This novel use of the RESET signal as recited in Claims 1 and 11 of the present invention provides functionality that is not possible with the use of an enabling signal such as the signal PMCPUCLKUNHALTED# 222 as disclosed in Chakravarthy.

It should be noted that Chakravarthy discloses a separate reset signal in paragraph 38 and Fig. 6 that is different from the enabling signal PMCPUCLKUNHALTED# 222. As taught in Chakravarthy, "this is done to prevent overflow." Thus, Chakravarthy resets the counter at the beginning of each calculation of CPU usage in order to prevent the counter from exceeding it's

maximum possible value. See Chakravarthy, Fig. 6. However, this reset does not occur each time a software task is running as is required in Claim 1 and 11 of the present invention. In fact, such a usage would render the invention in Chakavarthy useless, because it would not allow for an accurate calculation of the percentage of utilization of the CPU as is the purpose of Chakravarthy. See paragraph 2. In other words, Chakravarthy counts the number of clock cycles that occur during a given period of time regardless of whether the CPU is in continuous use or not, and the present invention counts the number of clock cycles during a particular phase of continuous usage, then automatically resets once the CPU becomes idle again. See Chakravarthy, ¶¶ 36-39.

Furthermore, Claims 1 and 11 include "[a] counter adapted to count the number of clock pulses since a RESET; the CPU adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU; and the monitor is adapted to store the value in the counter immediately prior to the last RESET." See Claims 1 and 11. By contrast, Chakravarthy requires a separate clock control unit 200.1 which is part of a BUS INTERFACE 200 to monitor a HLT signal 216 and a BREAK signal 218. See Chakravarthy, Figure 2. The clock control unit 200.1 must generate the PMCPUCLKUNHALTED# signal 222 and transmit it to a BUS UNIT PMON 200.2. *Id.* The BUS UNIT PMON 200.2 then pushes the PMCPUCLKUNHALTED# signal 222 out onto a PMON BUS 206 which communicates it to the performance monitor 204. *Id.*

Thus, an implementation as in claims 1 and 11, where "the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU" may eliminate the need for the HLT signal 216, the BREAK signal 218, BUS INTERFACE 200, clock control unit 200.1, bus unit PMON 200.2, and PMON bus 206 required to generate and communicate the PMCPUCLKUNHALTED# described in Chakravarthy. Therefore, Claims 1 and 11 are patentable over Chakravarthy, because Chakravarty fails to teach exactly what is claimed in each and every limitation of those claims.

Because Chakravarthy fails to teach each and every element recited in claims 1 and 11, the Office Action fails to establish a *prima facie* case of anticipation. Thus, Applicant respectfully submits that independent claims 1 and 11 are patentable over the cited reference.

Consequently, Applicant requests that the rejection of Claims 1 and 11 under 35 U.S.C. § 102(e) be withdrawn.

B. Dependent Claims 2-4 and 12-14

Given that dependent claims 2-4 depend from Claim 1 and Claims 12-14 depend from Claim 11, Applicant respectfully submits that those claims are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of dependent claims 2-4 and 12-14 under 35 U.S.C. § 102(e) be withdrawn.

**II. The Examiner failed to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a) because the cited references, either alone or in combination, do not teach or suggest all of the limitations of Claims 5-10 and 15-20.**

A. Dependent Claims 5-10 and 15-20

With regard to the rejection dependent Claims 5-10 and 15-20, Applicant respectfully submits that these claims are patentable as depending from allowable independent Claims 1and 11. Specifically, Chakravarthy fails to teach the recited element wherein "the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running." Accordingly, Applicant submits that claims 5-10 and 15-20 are patentable in their current form as depending from independent claims 1 and 11 respectively. Consequently, Applicant requests that the rejection of claims 5-10 and 15-20 under 35 U.S.C § 103(a) be withdrawn.

## SUMMARY

In view of the foregoing, each of the claims on appeal has been improperly rejected because the Examiner has not properly established a *prima facie* case of anticipation for Claims 1-4 and 11-14 in view of Chakravarthy, or a *prima facie* case of obviousness for Claims 5-10 and 15-20 in view of Chakravarthy combined with Terrell. Appellant submits that the foregoing arguments establish the novelty and non-obviousness of the claims of the present application. Therefore, Appellant respectfully requests reversal of the Examiner's rejection under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) and allowance of pending Claims 1-20. Accordingly, Appellant submits that Claims 1-20 are patentable.

Respectfully submitted,

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## 8. CLAIMS APPENDIX

The claims involved in the appeal are listed below.

1. A microprocessor system comprising a CPU, a clock providing a CLK signal to the CPU, a counter counting clock pulses to the CPU, and a monitor, wherein the clock is adapted to provide a CLK signal to the counter when a software task is running on the CPU, said counter adapted to count the number of clock pulses since a RESET; the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU; and the monitor is adapted to store the value in the counter immediately prior to the last RESET.

2. The microprocessor system of claim 1 wherein the CPU is adapted to block a RESET signal to the counter when a software task is running on the CPU.

3. The microprocessor system of claim 1 wherein the CPU is adapted to continuously pass CLK signals to the counter when a software task is running on the CPU.

4. The microprocessor system of claim 1 wherein the CPU is adapted to pass a RESET signal to the counter when is software task is not running on the CPU.

5. The microprocessor system of claim 1 wherein the monitor is adapted to output a control signal responsive to monitor content.

6. The microprocessor system of claim 5 wherein the monitor is adapted to output a power control signal responsive to monitor content.

7. The microprocessor system of claim 5 wherein the monitor is adapted to output a function control signal responsive to monitor content.

8. The microprocessor system of claim 5 wherein the monitor is adapted to output a clock

control signal responsive to monitor content.

9. The microprocessor system of claim 5 wherein the monitor is adapted to output a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold.

10. The microprocessor system of claim 5 wherein the monitor is adapted to output a control signal reducing clock pulse input to the CPU responsive to count content when the monitor content is below a threshold.

11. A method of operating a microprocessor system, said system comprising a CPU, a counter, a monitor, and a clock, and wherein the clock provides a CLK signal train to the counter while a software task is running on the CPU, the counter counting the number of clock pulses since a RESET, the CPU providing a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU, and the monitor storing the value of the counter prior to the last RESET.

12. The method of claim 11 wherein the CPU blocks the RESET signal to the counter when a software task is running on the CPU.

13. The method of claim 11 wherein the CPU continuously passes CLK signals to the counter when a software task is running on the CPU.

14. The method of claim 11 wherein the CPU passes a RESET signal to the counter when is software task is not running on the CPU.

15. The method of claim 11 wherein the monitor outputs a control signal responsive to count content.

16. The method of claim 15 wherein the monitor outputs a power control signal responsive to

monitor content.

17. The method of claim 15 wherein the monitor outputs a function control signal responsive to monitor content.

18. The method of claim 15 wherein the monitor outputs a clock control signal responsive to monitor content.

19. The method of claim 15 wherein the monitor outputs a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold.

20. The method of claim 15 wherein the monitor outputs a control signal reducing clock speed of the CPU responsive to monitor content when the monitor content is below a threshold.

## 9. EVIDENCE APPENDIX

There is no material to be included in the Evidence Appendix.

## 10. RELATED PROCEEDINGS APPENDIX

There is no material to be included in the Related Proceedings Appendix.